4. (Twice Amended) A LSI layout method for a LSI design by automatic arrangement wiring of standard cells, wherein logic gate cells and power supply capacitor cells are provided as the standard cells, comprising the operations of:

calculating a possible number of the power supply capacitor cells to be arranged based on a width of a dead space of the power supply and a width of the power supply capacitor cells, and

arranging the power supply capacitor cells in spaces of each block where standard cells are not arranged by the automatic arrangement wiring.